Novel Photodefined Polymer-Clad Through-Silicon Via Technology Integrated With Endpoint Detection Using Optical Emission Spectroscopy

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***Abstract*—Silicon interposers with through-silicon vias (TSVs) have been widely explored to obtain high density and high bandwidth communication between chips. To reduce TSV electrical loss and stress, novel photodefined polymer-clad TSVs are fabricated. Moreover, to reduce via under or over etching during TSV fabrication and accurately predict the endpoint for TSV etching, a hybrid partial least squares-support vector machine (PLS-SVM) model of optical emission spectroscopy (OES) data is successfully demonstrated. Accurate endpoint detection results are shown for 80 µm diameter TSVs.**

Keywords—3D integration; TSV; SU-8 cladding; optical emission spectroscopy; endpoint detection for Si DRIE etch

I. Introduction

The system performance gains from device scaling have been abating due to a host of challenges, including the slower rate of development in silicon ancillary technologies [1]. Moreover, the transition to multicore microprocessors has exacerbated the demand for off-chip bandwidth. These challenges have created a need for disruptive interconnect and packaging technologies to improve system performance. Silicon interposers with through-silicon vias (TSVs) and high density metallization have been widely explored as a novel system interconnect platform capable of providing high bandwidth-density communication between chips [2, 3]. However, there are electrical, thermomechanical and fabrication related challenges for TSVs in silicon interposers, including:

- Increasing the thickness of a silicon interposer minimizes warpage of large area interposers and possibly eases the assembly process, but it increases TSV length, leading to an increase in TSV capacitance and RF losses [4-6].
- Owing to the coefficient of thermal expansion (CTE) mismatch between the copper TSV and silicon, thermomechanical stress can be exerted on the TSVs, resulting in TSV reliability challenges [7].
- In TSV fabrication based on the Bosch process [8], either blind vias can be etched first in silicon followed by back side silicon polishing or vias can be etched through the entire thickness of silicon with a silicon dioxide layer at the base of the vias. In this paper, we focus on the latter approach. However, while implementing this approach, any changes to the process conditions result in run-to-run variations in etch rate leading to over or under etching of the vias for a fixed number of process cycles.

To address the electrical and thermomechanical challenges for TSVs in silicon interposers, novel polymer-clad TSVs were fabricated with a photodefined dielectric (polymer) liner [9], as shown in Fig. 1. Multilevel metallization can be built over the interposer with the novel TSVs and multiple chips can be interconnected atop the interposer. As the thickness of the TSV dielectric liner increases, TSV capacitance and RF losses decrease [10]. Additionally, a reduction in TSV stress can be attained using the polymer liner material [11, 12].

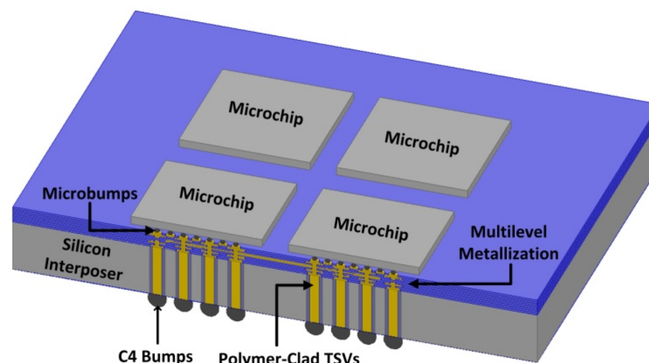


Fig. 1. Silicon interposer featuring polymer-clad TSVs and multiple interconnected chips with fine pitch multilevel metallization.

Moreover, to avoid via over or under etch and to control the critical dimensions of the TSVs by accurately predicting the endpoint for TSV etching, optical emission spectroscopy (OES) was used to monitor *in-situ* plasma process condition. The acquired OES data was analyzed using partial least squares (PLS) and support vector machines (SVM) [13, 14] to establish predictive endpoint detection models.

II. Polymer-Clad TSVs

Prior efforts in the fabrication of TSV polymer liners involved vapor deposition of polymer [15], polymer filling in circular trenches [16], laser ablation of polymer-filled vias [17], and photodefinition of polymer-filled vias with a

temporary release film [18]. This paper describes the fabrication of polymer-clad TSVs using photodefinition of polymer-filled vias with a mesh [19] at the base of the vias. SU-8 was used in this work since the high aspect-ratio photodefinition of SU-8 is a well-established process [20]. Investigation of other polymer materials is work in progress. To better illustrate the differences between the competing TSV liner fabrication techniques, Table 1 summarizes the benefits and limitations of each approach.

Table 1. Comparison of TSV liner fabrication methods.

	Principle	Benefit	Limitation
Silicon Dioxide	Thermal oxidation or PECVD	Easy for manufacturing	Limited cladding thickness
Vapor Deposition [15]	Deposition of parylene	Deposition at room temperature	Limited cladding thickness
Trench Polymer Filling [16]	Trench polymer filling followed by silicon etching	Wide selection of polymers is available	Filling in high aspect-ratio vias may be difficult
Laser Ablation [17]	Serial ablation of polymer filled in vias	Panel-scale fabrication possible	Serial process and precision of ablation
Photo-definition	Photodefinition of polymer-filled vias	Knowledge of high aspect-ratio photodefinition easily available in literature	Limited selection of high aspect-ratio photodefinable materials

As shown in Fig. 2, to fabricate the polymer-clad TSVs, a silicon dioxide layer was first deposited on one surface of a silicon wafer, followed by anisotropic etching of vias using the Bosch process. Next, a set of micro-vias (i.e. mesh pattern [19]) was etched in the silicon dioxide layer underneath the etched vias. Once the mesh was etched, SU-8 was coated to fill the etched vias followed by soft bake. The presence of mesh helps obtain void-free filling of SU-8 in the vias. Minor SU-8 leakage was observed from the mesh after soft bake. Next, ultraviolet (UV) exposure, post exposure bake, SU-8 development, and isopropanol clean were performed, yielding vias with thick cladding. Once the cladding was fabricated, titanium and copper seed layers were deposited over the silicon dioxide end of the wafer, followed by pinch-off of the fabricated silicon dioxide mesh with copper electroplating. Next, bottom-up copper electroplating was performed followed by chemical mechanical polishing (CMP) to remove overburden copper.

Using this fabrication process, 390 μm tall and 80 μm diameter copper vias on a 250 μm pitch were fabricated; the SU-8 cladding was 20 μm thick, as shown in Fig. 3(a). Void-free copper electroplating was obtained, as shown in the x-ray image (Fig. 3(b)) of the fabricated polymer-clad TSVs. Resistance of the fabricated TSVs was measured using the four-point method. The average measured value of 20 different TSVs was 2.81 mΩ. The deposition of barrier and adhesion layers over TSV sidewalls has been commonly demonstrated in literature for the conventional TSVs fabricated using superfill electroplating [21]; it can be adopted in the proposed polymer-clad TSVs.

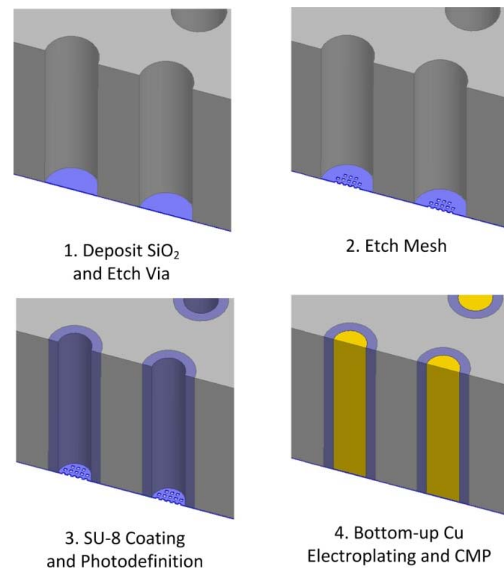


Fig. 2. Fabrication process for polymer-clad TSVs.

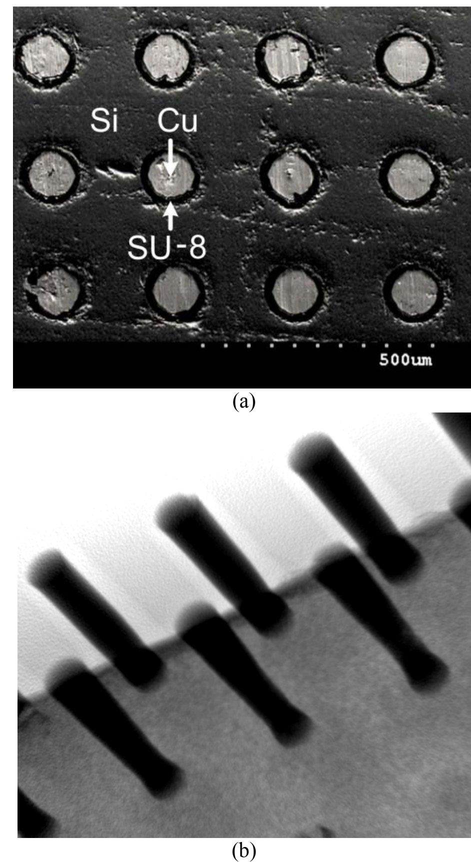


Fig. 3. (a) Top view and (b) x-ray image of 390 μm tall polymer-clad TSVs with 80 μm diameter copper vias surrounded by a 20 μm thick polymer cladding on a 250 μm pitch.

III. ENDPOINT DETECTION USING OES

For TSV fabrication using the Bosch process, vias are first etched through the silicon wafer to leave behind an oxide layer at the base of the vias. When the oxide layer at the base is reached while etching, positive ion accumulation occurs over the oxide. Consequently, the incoming positive ion flux is repelled from the accumulated ion layer and starts attacking the lower part of the via sidewall, resulting in notching at the base of the vias [8]. Fig. 4 shows an image of over etched 300 µm tall and 120 µm diameter vias on a 250 µm pitch. In order to avoid via over or under etch and thereby control the critical dimensions of TSVs, it is of significant importance to predict the endpoint during etching.

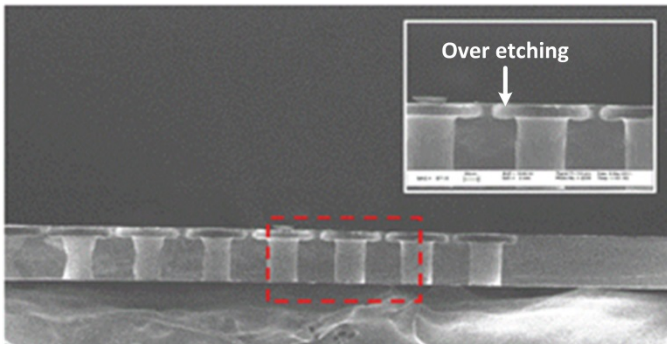


Fig. 4. Over etched 120 µm diameter TSVs.

Endpoint detection has been widely explored for the etching of various materials such as polymer films using Langmuir probe [22], blanket polysilicon using laser interferometry [23], and chrome dry-etching using RF sensor [24]. However, for silicon etching using the Bosch process, it is difficult to predict the endpoint since the Bosch process has time division multiplexed (TDM) etch and passivation cycles. R. Westerman et al. [25] demonstrated endpoint detection for the Bosch process silicon etching in a silicon-on-insulator (SOI) wafer by implementing an envelope follower algorithm using OES. However, the signals for demonstrating the envelope follower algorithm used both passivation and etch steps. Consequently, the envelope follower algorithm is influenced by the passivation step, where SiF_x intensity includes carbon noise from C_4F_8 (the passivation gas).

In contrast to past work in OES, this paper proposes a hybrid partial least squares-support vector machine (PLS-SVM) model of the OES data, as shown in Fig. 5, and successfully demonstrates the endpoint detection of 80 µm diameter TSVs with low open area. In this approach, only the etch step is used for endpoint detection, excluding the influence of the passivation step. Moreover, this approach specifically uses the SVM classification algorithm to accurately classify the signals before and after the endpoint. The steps of the proposed model in Fig. 5 are described as follows:

***Step 1*:** An optical emission sensor was mounted on top of the process chamber of the STS inductively coupled plasma (ICP) system, as shown in Fig. 6. The acquired OES data was analyzed after TSV etching. To alleviate wafer-to-wafer thickness variation, the etching was performed on one half of a wafer first while keeping the other half of the wafer covered. Once the etching of the first half was completed and an endpoint was predicted, the second half was etched to confirm the accuracy of the hybrid PLS-SVM model.

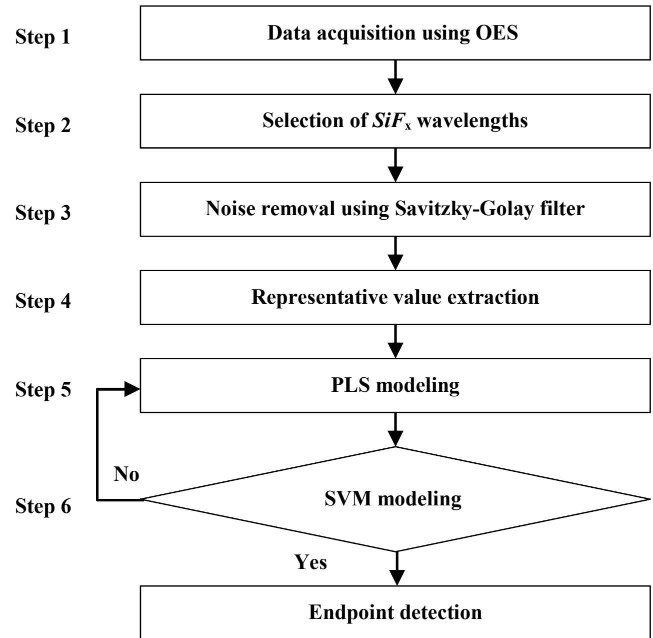


Fig. 5. Flowchart of the proposed hybrid PLS-SVM model.

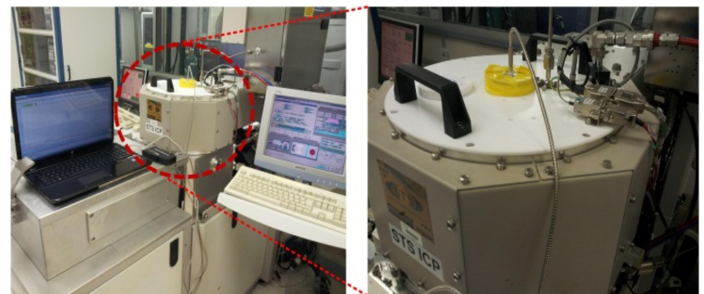
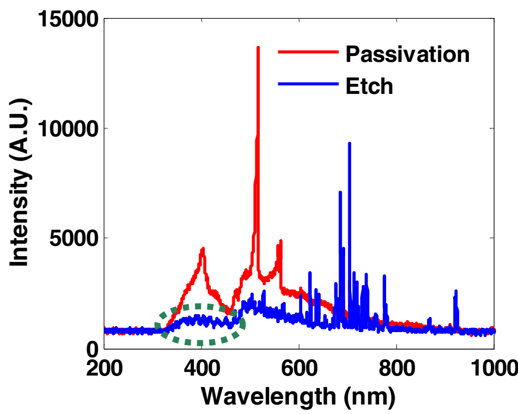
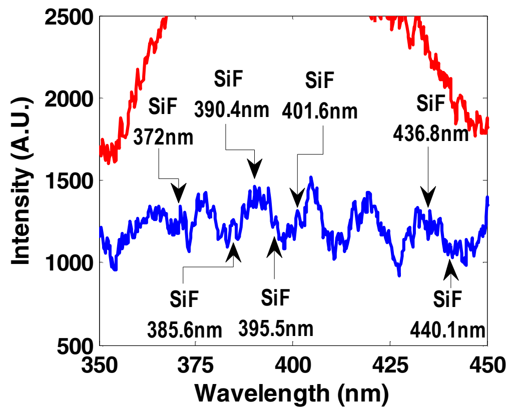


Fig. 6. Experimental setup for endpoint detection of TSVs using OES with the OES sensor mounted on top of ICP etching tool process chamber.

***Step 2*:** As shown in Fig. 7, during the Bosch process, multiple optical emission wavelengths related to the SiF_x group were identified with reasonable emission intensity changes around the TSV endpoint. Seven different optical emission wavelengths related to the SiF_x group were selected for data analysis.



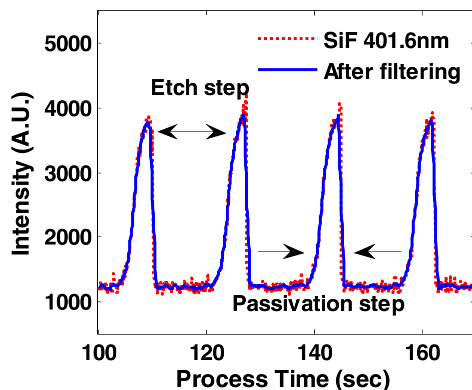
(a)



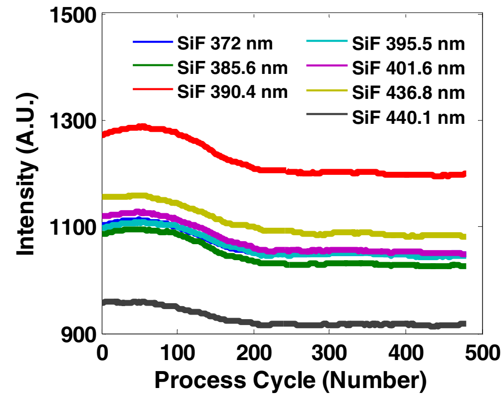
(b)

Fig. 7. (a) Passivation and etch step spectra for silicon etch process (the plasma emission spectra of both steps are different) and (b) Magnified image (green circle) of (a) (the selected SiF_x species in etch step during silicon etching).

***Steps 3 and 4*:** To identify a useful region in the data, the SiF_x OES signal was filtered by a Savitzky-Golay smoothing filter [26] to eliminate noise from the SiF_x related peaks. As shown in Fig. 8, the result of the Savitzky-Golay smoothing filter was extracted using the mean value in each etch cycle in order to generate the representative values of SiF_x for all etch cycles.



(a)



(b)

Fig. 8. (a) Filtered SiF_x intensity using the Savitzky-Golay smoothing filter, and (b) Mean integrated values of SiF_x intensity during etch cycles.

***Step 5*:** After filtering, PLS was applied to these representative values to generate an endpoint detection signal. PLS regression is based on principal component analysis (PCA) and is an extension of the NIPALS algorithm [27]. The main idea of PLS is to successively select directions of variation in the input data matrix that maximize the output variation that can be predicted. The input matrix is comprised of the generated mean representative value from seven SiF_x wavelengths, while the output matrix is constructed by the product of raw spectrum data and signal vectors around the endpoint. Once PLS was applied, the endpoint was apparent around 390th cycle for the 80 μm diameter TSVs, as shown in Fig. 9.

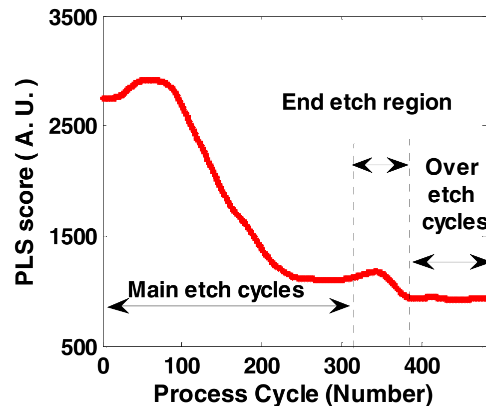


Fig. 9. The generated endpoint signal for 80 μm diameter TSVs from the first run of back-to-back etching using PLS

***Step 6*:** Next, an SVM model was established to classify the etch data into two classes (before and after endpoint) by constructing an *n*-dimensional hyper-plane. As shown in Fig. 10, using the hybrid PLS-SVM model, an accurate endpoint (390th cycle) was computed from over etching of the first half of a wafer while keeping the other half of the wafer covered. The computed endpoint was applied during the etching of the second half of the wafer, while covering the first half. Table 2

illustrates the average via diameters after the etching of each half of the wafer. Accurate endpoint detection was obtained for the etched 80 µm diameter TSVs. Fig. 11 illustrates bottom views and cross sectional views of the etched TSVs.

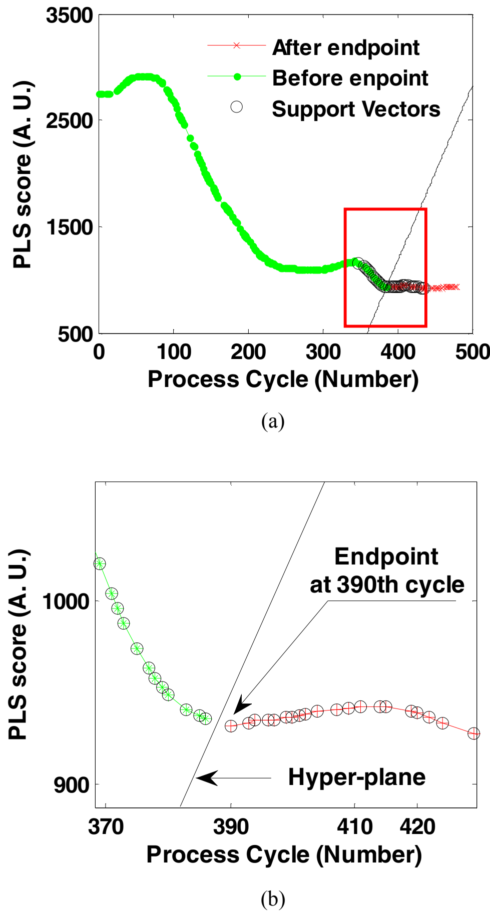
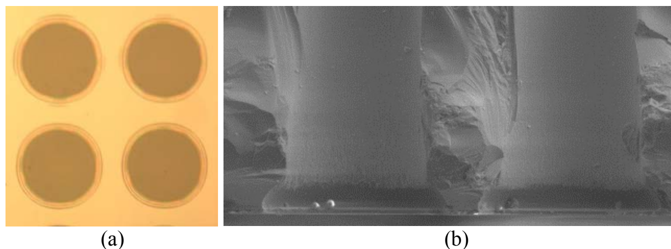


Fig. 10. (a) Endpoint prediction for 80 µm diameter TSVs by applying SVM and (b) Endpoint detection at 390th cycle.

Table 2. TSV etching results.

TSV Diam. (µm)	Wafer Half	Process Cycle	Average diameter for 100 vias (µm)		Variations between the maximum and the minimum diameters (µm)	
			Top	Bottom	Top	Bottom
80	1st	480	84.72	122.85	5.96	12.21
	2nd	390	83.11	79.54	3.98	6.54



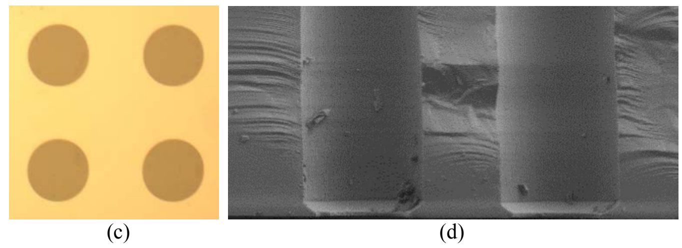


Fig. 11. (a) Bottom view, (b) Cross-sectional view of 80 µm diameter TSVs after etching the first half of a wafer for 480 cycles, (c) Bottom view, and (d) Cross-sectional view of 80 µm diameter TSVs after etching the second half of the wafer for 390 cycles as predicted endpoint.

IV. CONCLUSION

This paper demonstrates the fabrication of photodefined polymer-clad TSVs for improved electrical and mechanical performance. Moreover, this paper demonstrates an OES-based endpoint detection technique using a hybrid PLS-SVM model as a promising approach to control silicon via etching during the Bosch process etch and thereby obtain desired critical dimensions for TSVs.

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